

IN THE CLAIMS

What is claimed is:

1 1. A semiconductor device including an insulated gate field effect transistor (IGFET),
2 comprising:

3 a gate electrode of the IGFET having a lower layer electrode formed
4 on a gate insulating film and an upper layer electrode formed on the lower
5 layer electrode;
6 a cap film formed on the upper layer electrode;
7 a first nitride film on a side surface of the upper layer electrode;
8 an oxide film on a side surface of the lower layer electrode; and
9 an etching stopper film including a second nitride film formed on the
10 outside of the first nitride film and oxide film.

1 2. The semiconductor device according to claim 1, wherein:

2 first nitride film is a thermal nitride film.

1 3. The semiconductor device of claim 2, wherein:

2 first nitride film is a rapidly heated thermal nitride film.

1 4. The semiconductor device of claim 2, wherein:

2 the first nitride film has a film thickness of approximately 2 to 5 nm.

- 1 5. The semiconductor device of claim 2, further including:
 - 2 an interlayer insulating film formed to cover the gate electrode of the
 - 3 IGFET;
 - 4 a contact hole opened in the interlayer insulating film to expose a
 - 5 source/drain region of the IGFET; and
 - 6 a conductor filling the contact hole and electrically connected with the
 - 7 source/drain region.

- 1 6. The semiconductor device of claim 2, wherein:
 - 2 the oxide film is a thermal oxide film.

- 1 7. The semiconductor device of claim 2, wherein:
 - 2 the second nitride film is formed with chemical vapor deposition
 - 3 (CVD).

- 1 8. A method for manufacturing a semiconductor device including an insulated gate field
- 2 effect transistor (IGFET), comprising the steps of:
 - 3 forming a gate insulating film on a semiconductor substrate;
 - 4 forming a laminate film on the gate insulating film, the laminate film
 - 5 including an insulating film formed on a second conductive film formed on a
 - 6 first conductive film;
 - 7 etching the insulating film and second conductive film into a
 - 8 predetermined pattern to form a cap film and an upper layer gate electrode;

9 forming a first nitride film on the side surface of the upper layer gate
10 electrode;
11 etching the first conductive film using the cap layer, upper layer gate
12 electrode, and the nitride film as a mask to form a lower layer gate electrode;
13 forming a first oxide film on the side surface of the lower layer
14 electrode; and
15 forming an etching stopper film including a second nitride film over
16 the entire surface.

- 1 9. The method for manufacturing a semiconductor device of claim 8, wherein:
 - 2 the first conductive film includes a polysilicon film; and
 - 3 the second conductive film includes a metal film.
- 1 10. The method for manufacturing a semiconductor device of claim 8, wherein:
 - 2 the first conductive film includes a polysilicon film; and
 - 3 the second conductive film includes a metal silicide film having a high
 - 4 melting point.
- 1 11. The method for manufacturing a semiconductor device of claim 8, wherein:
 - 2 the first nitride film is a thermal nitride film; and
 - 3 the first oxide film is a thermal oxide film.
- 1 12. The method for manufacturing a semiconductor device of claim 8, wherein:

2 forming the etching stopper film includes forming the second nitride
3 film with a chemical vapor deposition.

1 13. The method for manufacturing a semiconductor device of claim 8, wherein:
2 the first nitride film is a thermal nitride film formed with a rapid
3 thermal nitridation step using a lamp as a heat source.

1 14. The method for manufacturing a semiconductor device of claim 8, further including
2 the steps of:

3 forming a source/drain region by doping an impurity into the
4 semiconductor substrate after the step of forming the first oxide film; and
5 forming an interlayer insulating film over the entire surface and
6 selectively etching the interlayer insulating film with a selective etching ratio
7 for the etching stopper film to open a contact hole after the step of forming the
8 etching stopper film.

1 15. The method for manufacturing a semiconductor device of claim 8, further including
2 the steps of:

3 forming a LDD (lightly doped drain) region by doping a first impurity
4 concentration into the semiconductor substrate after the step of forming the
5 first oxide film;
6 anisotropic etching the etching stopper film to form a side wall etching
7 stopper film on side surfaces of the lower layer gate electrode, upper layer

8 gate electrode and cap layer; and
9 forming a source/drain region by doping a second impurity
10 concentration into the semiconductor substrate using the side wall etching
11 stopper film as a mask wherein the first impurity concentration is lower than
12 the second impurity concentration.

1 **16.** The method for manufacturing a semiconductor device of claim 15, further including
2 the steps of:

3 forming a second oxide film over the entire surface of the substrate
4 with a chemical vapor deposition method;

5 anisotropic etching the second oxide film to form a side oxide film on
6 the side surface of the etching stopper film; and

7 forming the source/drain region after the step of forming the side wall.

1 17. A semiconductor device including a first region and a second region, comprising:

2 a first gate electrode of a first IGFET in the first region having a first
3 lower layer electrode formed on a first gate insulating film and a first upper
4 layer electrode formed on the first lower layer electrode;

5 a first cap film formed on the first upper layer electrode;

6 a first nitride film on a side surface of the first upper layer electrode:

7 a first oxide film on a side surface of the first lower layer electrode;

8 a first etching stopper film including a second nitride film formed on
9 the outside of the first nitride film and first oxide film;

10 a second gate electrode of a second IGFET in the second region having
11 a second lower layer electrode formed on a second gate insulating film and a
12 second upper layer electrode formed on the second lower layer electrode;
13 a second cap film formed on the second upper layer electrode;
14 a third nitride film on a side surface of the second upper layer
15 electrode;
16 a second oxide film on a side surface of the second lower layer
17 electrode;
18 a second etching stopper film including a fourth nitride film formed on
19 the outside of the third nitride film and second oxide film; and
20 wherein the first IGFET includes a lightly doped drain. *and the second region
drain and source
in 102*

1 18. The semiconductor device of claim 17, wherein:
2 the semiconductor device is a semiconductor memory device.

1 19. The semiconductor device of claim 18, wherein:
2 the first region is a memory cell region and the second region is a
3 peripheral circuit region.

1 20. The semiconductor device of claim 19, further including:
2 a first contact providing an electrical connection to a first source/drain
3 region of the first IGFET;
4 a second contact providing an electrical connection to a second

5 source/drain region of the second IGFET; and
6 a first spacing from the first contact to the first gate electrode is greater
7 than a second spacing from the second contact to the second gate electrode.